**WHAT IS CLAIMED IS:**

1. An apparatus comprising:

a first transistor having a first control terminal coupled to receive a first dynamic data signal, wherein the first transistor is coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the first dynamic data signal;

a second transistor coupled to the first node and having a second control terminal, the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal; and

a circuit coupled to generate the signal on the second control terminal and coupled to receive a second dynamic data signal, the second dynamic data signal being a complement of the first dynamic data signal, wherein the circuit is configured to activate the second transistor responsive to an assertion of the second dynamic data signal.

2. The apparatus as recited in claim 1 further comprising a first plurality of transistors, wherein the first transistor is one of the first plurality of transistors and wherein the first dynamic data signal is one of a first plurality of dynamic data signals, each of the first plurality of transistors having a control terminal coupled to receive a respective one of the first plurality of dynamic data signals, wherein each of the first plurality of transistors is coupled to the first node and is configured to drive the first state on the first node responsive to an assertion of the respective one of the first plurality of dynamic data signals, and wherein the circuit is coupled to receive a second plurality of dynamic data signals including the second dynamic data signal, wherein each of the second plurality of

dynamic data signals is a complement of a respective one of the first plurality of dynamic data signals, and wherein the circuit is configured to activate the second transistor responsive to an assertion of one of the second plurality of dynamic data signals.

3. The apparatus as recited in claim 2 wherein the circuit performs a logical NOR of the second plurality of dynamic data signals.

4. The apparatus as recited in claim 3 wherein the circuit is a NOR gate.

5. The apparatus as recited in claim 2 further comprising a second plurality of transistors, each having a control terminal coupled to receive a respective one of the second plurality of dynamic data signals, and each of the second plurality of transistors coupled to the first node.

6. The apparatus as recited in claim 5 wherein the second transistor is a PMOS transistor.

7. The apparatus as recited in claim 6 wherein the second plurality of transistors are each NMOS transistors.

8. The apparatus as recited in claim 7 wherein the first plurality of transistors are each NMOS transistors.

9. The apparatus as recited in claim 1 further comprising an inverter having an input coupled to the first node and driving an output signal representing the value represented by an asserted one of the first dynamic data signal or the second dynamic data signal.

10. The apparatus as recited in claim 1 further comprising a keeper coupled to the first node and configured to retain a previous state of the first node responsive to a deassertion

of each of the first dynamic data signal and the second dynamic data signal.

11. The apparatus as recited in claim 10 wherein the keeper is coupled to receive an indication of an evaluate phase of the first and second dynamic data signals, and wherein the keeper is inactive during the evaluate phase.

12. The apparatus as recited in claim 1 wherein the circuit comprises an inverter.

13. A memory array comprising:

a plurality of banks of memory, each bank configured to output a first dynamic data signal indicative of a bit stored in the bank and a second dynamic data signal indicative of the complement of the bit; and

a bank select circuit coupled to receive the first dynamic data signal and the second dynamic data signal from each of the plurality of banks and configured to output a selected bit responsive to the first dynamic data signal and the second dynamic data signal from each of the plurality of banks, the bank select circuit comprising:

a first plurality of transistors, each having a control terminal coupled to receive the first dynamic data signal from a respective one of the plurality of banks, wherein each of the first plurality of transistors is coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the first dynamic data signal;

a second transistor coupled to the first node and having a second control

terminal, the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal; and

a circuit coupled to generate the signal on the second terminal and coupled to receive the second dynamic data signal from each of the plurality of banks, wherein the circuit is configured to activate the second transistor responsive to an assertion of the second dynamic data signal from one of the plurality of banks.

14. The memory array as recited in claim 13 further comprising a decoder coupled to each of the plurality of banks, wherein the decoder is configured to activate at most one of the plurality of banks to output data via the first dynamic data signal or the second dynamic data signal.

15. The memory array as recited in claim 13 wherein the bank select circuit further comprises an inverter having an input coupled to the first node and a driving the selected bit output from the bank select circuit.

16. The memory array as recited in claim 13 wherein the bank select circuit further comprises a keeper coupled to the first node and configured to retain a previous state of the first node responsive to a deassertion of each of first dynamic data signals and the second dynamic data signals.

17. The memory array as recited in claim 13 wherein the circuit performs a logical NOR of the second dynamic data signals from each of the plurality of banks.

18. The memory array as recited in claim 17 wherein the circuit is a NOR gate.

19. The memory array as recited in claim 13 wherein the bank select circuit further comprises a second plurality of transistors, each having a control terminal coupled to receive the second dynamic data signal from a respective one of the plurality of banks, and each of the second plurality of transistors coupled to the first node.

20. The memory array as recited in claim 19 wherein the second transistor is a PMOS transistor.

21. The memory array as recited in claim 20 wherein the second plurality of transistors are each NMOS transistors.

22. The memory array as recited in claim 21 wherein the first plurality of transistors are each NMOS transistors.

23. A computer accessible medium comprising one or more data structures representing:

a first plurality of transistors, each having a control terminal coupled to receive a respective one of a first plurality of dynamic data signals, wherein each of the first plurality of transistors is coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the respective one of the first plurality of dynamic data signals;

a second transistor coupled to the first node and having a second control terminal, the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal; and

a circuit coupled to generate the signal on the second terminal and coupled to

receive a second plurality of dynamic data signals, each of the second plurality of dynamic data signals being a complement of a respective one of the first plurality of dynamic data signals, wherein the circuit is configured to activate the second transistor responsive to an assertion of one of the second plurality of dynamic data signals.

24. The computer accessible medium as recited in claim 23 wherein the one or more data structures further represent a memory array, the memory array comprising:

a plurality of banks of memory, each bank configured to output a first dynamic data signal indicative of a bit stored in the bank and a second dynamic data signal indicative of the complement of the bit; and

a bank select circuit coupled to receive the first dynamic data signal and the second dynamic data signal from each of the plurality of banks and configured to output a selected bit responsive to the first dynamic data signal and the second dynamic data signal from each of the plurality of banks, the bank select circuit comprising the first plurality of transistors, the second transistor, and the circuit.

25. A computer accessible medium comprising one or more data structures representing:

a first transistor having a first control terminal coupled to receive a first dynamic data signal, wherein the first transistor is coupled to a first node and is configured to drive a first state on the first node responsive to an assertion of the first dynamic data signal;

a second transistor coupled to the first node and having a second control terminal,

the second transistor configured to drive a second state on the first node responsive to a signal on the second control terminal; and

a circuit coupled to generate the signal on the second control terminal and coupled to receive a second dynamic data signal, the second dynamic data signal being a complement of the first dynamic data signal, wherein the circuit is configured to activate the second transistor responsive to an assertion of the second dynamic data signal.